22/9/1 **(Item 1 from file: 348)**
DIALOG®File 348:EUROPEAN PATENTS

01034850
Image forming apparatus
Bilderzeugungsgerat
Appareil de formation d'image
PATENT ASSIGNEE:
KONICA CORPORATION, (206976), 26-2 Nishishinjuku 1-chome, Shinjuku-ku, Tokyo, (JP), (Applicant designated States: all)
INVENTOR:
Deguchi, Takashi, c/o Konica Corporation, 1 Sakura-machi, Hino-shi, Tokyo , (JP)
Kawabe, Toru, c/o Konica Corporation, 1 Sakura-machi, Hino-shi, Tokyo, (JP)
Hattori, Tuyosi, c/o Konica Corporation, 1 Sakura-machi, Hino-shi, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Nicholls, Michael John (61941), J.A. KEMP & CO. 14, South Square Gray's Inn, London WC1R 5LX, (GB)
PATENT (CC, No, Kind, Date): EP 920191 A2 990602 (Basic)
EP 920191 A3 000531
APPLICATION (CC, No, Date): EP 98309636 981125;
PRIORITY (CC, No, Date): JP 97343794 971128

DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04N-001/40

ABSTRACT EP 920191 A2

There is described an image recording apparatus, which includes an input device for inputting image data, a recording element to record images on an image recording medium in accordance with the image data, a memory device for storing a plurality of information groups having relationship between image data and recording energy control data, a discriminator for discriminating a sort of the image recording medium, a selector for selecting at least one information group out of the plural information groups in accordance with the sort of the image recording medium discriminated by the discriminator, and a controller for controlling the recording element on the basis of the information group selected by the selector.

ABSTRACT WORD COUNT: 113
NOTE:
Figure number on first page: 1A

LEGAL STATUS (Type, Pub Date, Kind, Text):
Search Report: 000531 A3 Separate publication of the search report
Application: 990602 A2 Published application (A1with Search Report ;A2without Search Report)
Examination: 001227 A2 Date of request for examination: 20001102
Change: 991124 A2 Inventor information changed: 19991007
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9922	659
SPEC A	(English)	9922	15105
Total word count - document A			15764
Total word count - document B			0
Total word count - documents A + B			15764

SPECIFICATION

BACKGROUND OF THE INVENTION

The present invention relates to an image forming apparatus which forms an image on a recording material by employing a recording element, and more particularly, to an image forming apparatus having therein a storage means that stores plural recording energy control data (hereinafter, referred to as recording energy control units), a discriminator means for discriminating the kinds of recording materials and means for switching a setting of the recording energy control units based on information discriminated by the discriminator means.

In an image recording apparatus wherein a silver halide photosensitive material is subjected to exposure and recording in accordance with image information, there is known a system employing a print head (array-type head) in which a plurality of recording elements (light sources) are arrayed in a line, as a method having various merits such as low cost, a compact apparatus, a easiness to obtain high quantity output, etc.

There has been proposed an apparatus wherein a vacuum fluorescent tube light source called VFPH (Vacuum Fluorescent Print Head) is used as the print head, stated above. The vacuum fluorescent tube light source has special features such as easily obtained high luminance, quick response and a slim body. By the way, a zinc oxide phosphor is selected as a

Next, circuits inside the green light-use recording head 51 and the blue light-use recording head 61 will be explained according to Fig. 6 which is a circuit diagram of the circuits inside the recording heads 51 and 61. The recording heads 51 and 61 have therein shift registers 111 - 118, latch circuits 121, 122, gates 131, 132, and a recording head 140. A signal receiving section 71 receives 1 bit serial image data AL1, AL2, AL3, AL4, AR1, AR2, AR3, AR4, the latch control signal LOAD, output control signals ESTBR, ESTBL, and the clock signal for data shift CLK from the signal processing circuit of the signal processing section 10, and supplies them to each section as shown in Fig. 6.

Then, 1 bit serial data AR1 is set to the shift register 111, 1 bit serial data AR2 is set to the shift register 112, 1 bit serial data AR3 is set to the shift register 113, 1 bit serial data AR4 is set to the shift register 114, 1 bit serial data AL1 is set to the shift register 115, 1 bit serial data AL2 is set to the shift register 116, 1 bit serial data AL3 is set to the shift register 117, and 1 bit serial data AL4 is set to the shift register 118, in timed relationship with the clock signal CLK for data shift.

The latch circuit 121 latches 1 bit serial image data AR1 - AR4 which are set to shift registers 111 - 114, according to the latch control signal LOAD. The latch circuit 122 latches 1 bit serial data AL1 - AL4 which are set to shift registers 115 - 118, according to the latch control signal LOAD.

A gate 131 generates 1 bit driving signal of L or H from the output control signal ESTBR for each light emitting section, according to 1 bit serial image data latched by the latch circuit 121, and sends it to the recording head 140. A gate 132 generates 1 bit driving signal of L or H from the output control signal ESTBL in accordance with paper information for each light emitting section, according to 1 bit serial image data latched by the latch circuit 122, and sends it to the recording head 140. The recording head 140 drives each light emitting section by the driving signals generated by gates 131 and 132.

Incidentally, the output control signal ESTBL is 1 bit signal of H or L, and the gate 132 is driven by 1 bit serial image data when the output control signal ESTBL is H, and generates the driving signal of all L when the output control signal ESTBL is L. In the same manner, the output control signal ESTBR is 1 bit signal of H or L, and the gate 131 is driven by 1 bit serial image data when the output control signal ESTBR is H, and generates the driving signal of all L when the output control signal ESTBR is L. ESTBL or ESTBR **selects** the **optimum time** for the paper registered in advance on a signal generation control section.

Next, each signal processing circuit for green light and blue light of the signal processing section 10 which generates from inputted image signal, 1 bit serial image data AL1, AL2, AL3, AL4, AR1, AR2, AR3, AR4, the larch control signal LOAD, output control signals ESTBR, ESTBL, and clock signal CLK for data shift, which are sent to the green light-use and blue light-use recording heads 51 and 61, will be explained according to Fig. 7 which is an outline block diagram of the image processing section 10.

The signal processing circuit has a multiplier 11 to multiply correction data and image data sent from the image processing control circuit 1, in order to correct unevenness of light emitting characteristics of each light emitting section of the recording head; a correction data memory 12 to store the correction data sent from the image processing control circuit 1 and to supply it to the multiplier 11; a correction control section 13 to receive the control signal from the image processing control circuit 1 and the status signal of the memory